

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor unit having two device terminals for every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface;  
and  
a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate ~~through said input/output pad with said input/output pad contacting said main surface of said laminated substrate,~~  
~~wherein said two device terminals [[being]] are mounted on said laminated substrate and [[being]] connected to both ends of a signal wire in said signal wiring layer, and said laminated substrate further comprises a via hole, with one end thereof connected to said signal wire and the other end thereof connected to said input/output pad of said semiconductor chip said signal wire being connected to the input/output pad of said semiconductor chip through a via hole formed in said laminated substrate.~~

2. (Original) A semiconductor unit as claimed in claim 1, wherein said semiconductor chip comprises an input/output circuit corresponding to said input/output pad, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element.

3-4. (Cancelled)

5. (Original) A semiconductor unit as claimed in claim 1, wherein said signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip.

6. (Cancelled)

7. (Original) A semiconductor unit as claimed in claim 1, wherein said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer.

8-10. (Cancelled)

11. (Original) A semiconductor unit as claimed in claim 2, wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said semiconductor unit with a relationship as follows:

$$2 \times 2L \times 7\text{ns/m} < \text{tck}/10.$$

12. (Cancelled)

13. (Original) A semiconductor module comprising:

    a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface; and  
    a plurality of semiconductor units being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of semiconductor units being connected to said intra-module wires,

    each of said semiconductor units having two device terminals every one input/output signal, each of said semiconductor units comprising:

        a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

        a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

        said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole,

        one pair of said two device terminals in two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively.

14. (Original) A semiconductor module as claimed in claim 13, wherein said semiconductor chip comprises an input/output circuit corresponding to said input/output pad, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element.

15-16. (Cancelled)

17. (Original) A semiconductor module as claimed in claim 13, wherein said signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip.

18. (Cancelled)

19. (Original) A semiconductor module as claimed in claim 13, wherein said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer.

20-22. (Cancelled)

23. (Original) A semiconductor module as claimed in claim 14, wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said semiconductor unit with a relationship as follows:

$2 \times 2L \times 7\text{ns}/\text{m} < \text{tck}/10$ .

24. (Cancelled)

25. (Original) A semiconductor module as claimed in claim 13, wherein said module substrate comprises at least two wiring layers.

26-30. (Cancelled)

31. (Original) A semiconductor module as claimed in claim 13, wherein said semiconductor units comprise memory devices.

32-34. (Cancelled)

35. (Original) A semiconductor module as claimed in claim 31, wherein said semiconductor module further comprises a register, a control wiring between said register and a plurality of memory devices passing through between said two device terminals.

36-67. (Cancelled)

68. (Currently Amended) A semiconductor unit ~~as claimed in claim 61, comprising:~~  
a laminated substrate comprising at least two wiring layers including a signal wiring layer  
and a power supply or a ground wiring layer, said laminated substrate having a main surface and a

back surface:

two semiconductor chips each having an input/output pad, said semiconductor chips being mounted on the main surface and the back surface of said laminated substrate, respectively; and wherein said semiconductor unit further has different four device terminals for every one input/output signal every at least one signal, first and second terminals in said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at left side opposite to each other, third and fourth terminals of said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at right side opposite to each other, said first and said second terminals and said third and said fourth terminals being disposed at left and right of said laminated substrate opposite to each other, said first and said second terminals being connected to each other through a first via hole, said third and said fourth terminals being connected to each other through a second via hole, said first and said second via holes being connected to a corresponding signal pad of said semiconductor chip by a wire, respectively[.]]

wherein the first via hole, the second via hole and the wire are formed in said laminated substrate.

69-73. (Cancelled)

74. (Previously Presented) A semiconductor unit having two device terminals for every one input/output signal, said semiconductor unit comprising:

    a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface;

and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole,

wherein said semiconductor chip comprises an input/output circuit corresponding to said input/output pad, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element, and

wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said semiconductor unit with a relationship as follows:

$$2 \times 2L \times 7\text{ns/m} < \text{tck}/10.$$